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IN THE U.S. PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of:

APPLICANTS: Antti Ruha et al.

SERIAL NO.: 10/005,766 FILING DATE: 11/02/2001

EXAMINER: Pablo N. Tran ART UNIT: 2685

ATTORNEY'S DOCKET NO.: 872.0100.U1(US)

TITLE: MULTI-MODE I/O CIRCUITRY SUPPORTING LOW INTERFERENCE SIGNALING SCHEMES FOR HIGH SPEED DIGITAL INTERFACES

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AMENDED APPELLANT'S BRIEF ON APPEAL

This Amended Appeal Brief is being submitted in response to the Notification of Non-Compliant Appeal Brief mailed August 23, 2006, regarding an appeal from the Final Office Action mailed November 30, 2005.

If there are any deficiencies in payment, please charge deposit account no.: 50-1924 for any deficiency.

(1) REAL PARTY IN INTEREST

The real party in interest (RPI) is Nokia Corporation of Espoo Finland, as indicated in an assignment of the U.S. application.

(2) RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences of which the undersigned representative and assignee/RPI are aware that will directly affect, be directly affected by or have a bearing on the Board's decision in this appeal.

(3) STATUS OF CLAIMS

Claims 1-24 and 39-51 are pending in this appeal with claims 1, 2, 5-14, 17-24, 39, 40 and 43-51 standing finally rejected. Claims 25-38 were withdrawn from consideration. Claims 1-24 and 39-51 are reproduced in an Appendix accompanying this Brief as those claims stood finally rejected and objected to by a final Office Action dated November 30, 2005.

(4) STATUS OF AMENDMENTS

A Response under 37 C.F.R. §1.116 was submitted subsequent to the Final Rejection dated November 30, 2005. The Response under 37 C.F.R. §1.116 was filed on February 17, 2006, and made argument but no claim amendments. An Amendment was filed March 30, 2006 wherein claims 2, 14, and 40 were amended.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Reference may be had to FIGS. 1-4, 5a, and 5b for this Summary. Independent claim 1 is directed to a multi-mode Input/Output (I/O) circuit (10) for transmitting and receiving data between integrated circuits (ICs) (1, 2, and 3 of Fig. 1), wherein each IC contains at least one of said I/O circuits, comprising at least one of transmitter circuitry (12) or receiver circuitry (14), said transmitter circuitry sending data to receiver circuitry in another IC, and said receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors (Fig. 3,

generally) that are selectively interconnected together by switches (s1-s12 of Fig. 3) to operate as two single-ended (w1,w2 of Fig. 5a), current or voltage mode links, and as a single differential current or voltage mode link (w1, w2 of Fig. 5b).

Independent claim 13 is directed to a method for transmitting and receiving data between integrated circuits (ICs) (1, 2, and 3 of Fig. 1) that comprise a portable radio communication device, comprising providing at least two ICs to each contain at least one I/O circuit, said I/O circuit comprising at least one of transmitter circuitry (12) or receiver circuitry (14), the transmitter circuitry sending data to receiver circuitry in another IC, and the receiver circuitry receiving data from transmitter circuitry in another IC, the I/O circuit being constructed with CMOS-based transistors (Fig. 3, generally) and selectively interconnecting together the CMOS-based transistors with switches (s1-s12 of Fig. 3) to operate as two single-ended (w1,w2 of Fig. 5a), current or voltage mode links, and as a single differential current or voltage mode link (w1, w2 of Fig. 5b).

Independent claim 39 is directed to a device comprising a plurality of integrated circuits (ICs) (1, 2, and 3 of Fig. 1) and further comprising multi-mode Input/Output (I/O) circuit for transmitting and receiving data between at least two ICs, where each of the at least two ICs contains at least one of said I/O circuits, comprising at least one of transmitter circuitry (12) or receiver circuitry (14), the transmitter circuitry sending data to receiver circuitry in another IC, and the receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors (Fig. 3, generally) that are selectively interconnected together by switches (s1-s12 of Fig. 3) to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link (w1, w2 of Fig. 5b).

Dependent claims 2, 14 and 40 are directed an I/O circuit, a method, and a device wherein said transmitter circuitry (12) sends data to said receiver circuitry (14) in another

IC over a first pair of adjacently disposed conductors (Fig. 1, "digital links"), and where said receiver circuitry receives data from said transmitter circuitry in another IC over a second pair of adjacently disposed conductors (Fig. 1, "digital links").

Dependent claims 6-11 are directed to a multi-mode I/O circuit wherein the transmitter circuitry and the receiver circuitry are selectively configured by switches for operating in a double single-ended voltage mode link mode (w1, w2 of Fig. 5A)(in claim 6), in a double single-ended current mode link mode (in claim 7), in a mode defined by a single differential voltage mode link with a single-ended input drive (in claim 8), in a mode defined by a single differential voltage mode link with a differential input drive (in claim 9), in a mode defined by a single differential current mode link with a single-ended input drive mode (in claim 10), and in a mode defined by single differential current mode link with a differential input drive (in claim 11). Dependent claims 17-22 correspond, generally, to claims 6-11 while being directed to a method for transmitting and receiving data between integrated circuits. Dependent claims 17-22 correspond, generally, to claims 44-49 while being directed to a device.

Dependent claim 5 is directed to a multi-mode I/O circuit as in claim 1, wherein the transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages (page 16, line 25). Dependent claim 23 corresponds, generally, to claim 5 while being directed to the method of claim 13. Dependent claim 43 corresponds, generally, to claim 5 while being directed to the device of claim 39.

Dependent claim 12 is directed to a multi-mode I/O circuit as in claim 1, wherein certain switches (s1-s12 of Fig. 3) are provided to convert said I/O circuitry into either

said transmitter circuitry configuration or into said receiver circuitry configuration.

Dependent claim 24

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The first ground for rejection (Issue A) presented for review by the Board is the propriety of the Examiner's rejection of claims 1-2, 5-6, 8-9, 12-14, 17, 20, 23-24, 39-40, 43-44, and 46-47 under 35 USC 102(b) as being anticipated by Hedberg (5,994,921).

B. The second ground for rejection (Issue B) presented for review by the Board is the propriety of the Examiner's rejection of claims 7, 10-11, 18-19, 21-22, 45, 48-49, and 51 as being unpatentable over Hedberg in view of Pena-Finol (5,832,370).

C. The third ground for rejection (Issue C) presented for review by the Board is the propriety of the Examiner's rejection of claims 2, 14 and 40 as providing insufficient antecedent basis for a limitation in the claim.

(7) ARGUMENT

ISSUE A:

ARGUMENT 1: HEDBERG DOES NOT DISCLOSE AN I/O CIRCUIT CONSTRUCTED WITH CMOS-BASED TRANSISTORS THAT ARE SELECTIVELY INTERCONNECTED TOGETHER BY SWITCHES TO OPERATE AS TWO SINGLE-ENDED, CURRENT OR VOLTAGE MODE LINKS, AND AS A SINGLE DIFFERENTIAL CURRENT OR VOLTAGE MODE LINK AS RECITED IN INDEPENDENT CLAIMS 1, 13, AND 39.

In the final Office Action, the Examiner rejected claims 1-2, 5-6, 8-9, 12-14, 17, 20, 23-24, 39-40, 43-44, and 46-47 as being anticipated by Hedberg. The standard for anticipation under 35 USC §102 is one of strict identity. To anticipate a claim for patent, a single prior source must contain all of the claim's elements. (See *Herman v. William Brooks Shoe Co.*, 54 USPQ2d 1046 (S.D. N.Y. 2000)).

With respect to claim 1, the Examiner asserted in the final Office Action that Hedberg discloses " a multi-mode Input/Output circuit for transmitting and receiving data between integrated circuits wherein each IC contains at least one of said I/O circuits having at least one of transmitter circuitry (fig. 5/no. 21, fig. 6/no. 21) and receiver circuitry (fig. 6/ no. 22), the IC are constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, voltage mode links, and as a single differential voltage mode link (fig. 5, fig. 6, col.1/ln. 15-29, col. 5/ln. 42-col. 6/ln. 8)."

Appellants respectfully assert that Hedberg does not teach an I/O circuit constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link as recited in independent claim 1.

With specific regards to claim 1, the Examiner's citations are examined as follows. At col. 1/lns. 15-29 of the Background section of Hedberg, it is stated:

> Advances in electronic technology and design, and a strive [sic] towards boosted performance in terms of power consumption and speed, among many other things, has led to a variety of concepts for electrical binary signaling between circuits and circuit boards. Early concepts are DTL (Diode-Transistor Logic), TTL (Transistor-Transistor Logic) and ECL (Emitter Coupled Logic). These employ so called single-ended signalling. More recent concepts often employ a technique called differential signalling, also known as balanced signalling, which uses two signalling wires. Such concepts are DPECL (Differential Pseudo Emitter Coupled Logic), LVDS (Low Voltage Differential Signalling) and GLVDS (Grounded Low Voltage Differential Signalling)

As is evident, Hedberg states, while discussing prior art, that previous attempts at electrical signaling employed single-ended signaling, while more recent attempts employ differential signaling. There is no teaching of a single circuit selectively inter-connectable to operate in either a single-ended mode or a differential mode as claimed. It is of further note that, in the Summary section, Hedberg states that "A sender device according to the invention is compatible with receiver devices of several existing signalling concepts, e.g. DPECL, LVDS and GLVDS." Every mention of compatible receiver devices involves a differential signaling regime as mentioned above.

At the Examiner's citation of col. 5/ln. 42-col. 6/ln. 8, there is provided a description of aspects of Figs. 5 and 6. Specifically, there are discussed two alternative approaches "for achieving appropriate supply voltages V_{BH}, V_{BL}, determined by the receiver entity 22, for the sender device 1." As disclosed at col. 3, lines 41-44, "The voltages at the outputs OUTP, OUTN are set by appropriately choosing the supply voltages VBH, VBL, which will be further described." At col. 3, lines 54-61, there are disclosed the voltage values for VBH and VBL compatible with signaling voltages of a DPECL receiver, a LVDS receiver, and a GLVDS receiver. As noted above, all of these receiver types comprise differential signaling concepts. As is clear from the Figs. 5 and 6, and the text of the specification, Hedberg teaches embodiments of the invention directed only to a sender device capable of sending digital information in the form of electrical binary signals to a receiver device using differential signaling.

This fact is nowhere more clearly stated than at the concluding paragraph of the specification at col. 6, lines 9-18, where it is stated:

> Various alterations and modifications can be done in the described embodiments of the invention by one having skills in the art, without departing from the scope and the spirit of the invention. For example, voltage values stated in the embodiments are only intended as examples for demonstrating the principles of the invention. Other voltage values may be used without changing the essentials of the invention. **Major principles of the invention apply also to single-ended sender devices. Single-ended signalling is well known in the art.** (emphasis added).

The highlighted portion of the text above comprises the only other recitation of "single-ended signaling" in the entire disclosure of Hedberg with the exception of the previously noted sentence in the Background section wherein it is stated "Advances in electronic technology and design, and a strive towards boosted performance in terms of power consumption and speed, among many other things, has led to a variety of concepts for electrical binary signaling between circuits and cicuit boards ... These employ so called single-ended signalling."

It is therefore evident that Hedberg nowhere teaches, or otherwise discloses, a sender device and a receiver device sending and receiving data via any method other than one employing differential signaling. Hedberg's mere assertion that "principles of the

invention apply to single-ended sender devices" is most certainly not a teaching that the receiver device and the sending device are "selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link" as recited in independent claim 1.

In the Advisory Action of March 14, 2006, the Examiner asserted "Further, Hedberg disclose such transmit/receive I/O circuits (fig. 5-6) that selectively inter-connectable to operate in either single-ended, voltage mode or differential voltage mode (col. 1/ln. 15-48, col. 2/ln. 7-28, **especially col. 2/ln. 22-28**)(emphasis added). The citation to col. 1/lns. 15-29 is discussed above. The additional citation to col. 1/lns 30-48 recites, generally, the typical low signaling voltage levels for various differential signaling schema and begins, "Although the above mentioned differential signaling concepts are indeed differential, each of the two signaling wires operate at fixed nominal voltages ...". There is no teaching that the two signaling wires can "operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link" as recited in claim 1.

The Examiner placed emphasis on the disclosure of col. 2/lns. 22-28 (stating "**especially col. 2/ln. 22-28**") as substantiating the assertion that Hedberg teaches "such transmit/receive I/O circuits (fig. 5-6) that selectively inter-connectable to operate in either single-ended, voltage mode or differential voltage mode". Appellants respectfully assert that Hedberg teaches no such thing. There is stated at col. 2, lines 22-28:

> A sender device according to the invention is compatible with receiver devices of several existing signalling concepts, e.g. DPECL, LVDS and GLVDS. The sender device according to the invention is also believed to be compatible with future signalling concepts. Signalling voltages of the sender device range from slightly negative, e.g. -0.5 V, up to in the order of several volts, e.g. 5 V.

As is evident, Hedberg makes specific reference to only differential signaling concepts, specifically, DPECL, LVDS, and GLVDS. In addition, as discussed above, Hedberg teaches choosing supply voltages, V_{BH} and V_{BL}, such that the two differential signaling output voltages, V_{OUTP} and V_{OUTN}, will be compatible with different differential signaling concepts. For example, Hedberg states at col. 3, lines 54-56, "By choosing for

example V_{BH} =3.9 V and V_{BL} =3.4 V, the output voltages V_{OUTP} and V_{OUTN} will be compatible with signalling voltages of a DPECL receiver ...".

It must further be noted that the Examiner misstates the recitation of claim 1 when citing to col. 2, lines 22-28. Specifically, claim 1, in addition to reciting that the CMOS-based transistors are selectively interconnected to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link, also recites that the CMOS-based transistors are selectively interconnected together **by switches** to so operate. (emphasis added). The Examiner makes no mention of the recitation of switches in claim 1.

As noted above, while Hedberg makes no disclosure of an I/O circuit comprising transistors that are selectively interconnected together to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link, what changes in operation of the transmitters and receivers that are taught are the result of choosing and supplying different supply voltages – not the selective interconnection of CMOS-based transistors by switches as recited in claim 1.

For this reason alone, the rejection of claim 1 must be withdrawn. As both of independent claims 13 and 39 likewise recite language similar to that discussed above with regards to claim 1, the rejections of claims 13 and 39 must likewise be withdrawn.

The Examiner rejected claims 5-6, 12, 17, 23-24, 39, 43-44 while citing the same citations as those asserted with respect to independent claims 1, 13, and 39. With regards to claims 5 and 6, both claims recite that the transmitter circuitry and the receiver circuitry "are selectively configured by switches for operating" in various modes. As noted above, Hedberg does not teach CMOS-based transistors selectively interconnected together by switches. As a result, Hedberg likewise does not teach transmitter and receiver circuitry selectively configured by switches for operating in the recited modes of claims 5 and 6. For this reason alone, the rejections of claims 5 and 6 must be withdrawn. Both claims 43 and 44, directed to the device of claim 39, similarly recite that the transmitter circuitry and the receiver circuitry "are selectively configured by switches for operating" in the same modes as recited in claim 5 and 6. Therefore, for the reasons discussed above, the rejections of claims 43 and 44 must be withdrawn.

Claim 12 recites "certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration." As noted above, Hedberg does not teach the selective configuration of switches to change

the mode of operation of the transmitter and receiver circuitry. Not surprisingly, Hedberg further does not teach converting the I/O circuitry into either a transmitter circuitry configuration or a receiver circuitry configuration via the provision of switches. Therefore, the rejection of claim 12 must be withdrawn. Claim 24 recites language similar to that of claim 12 and, for the reasons stated above, the rejection of claim 12 must likewise be withdrawn.

Claim 17 recites that the transmitter circuitry and the receiver circuitry "are selectively configured by the switches for operating in a double single-ended voltage mode link mode". As noted above, Hedberg does not teach the selective configuration of switches to operate the transmitter and receiver circuitry in a recited mode. As a result, the rejection of claim 17 must be withdrawn. Claim 23 recites that the transmitter circuitry and the receiver circuitry "are selectively configured by said switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages." As noted above, Hedberg does not teach the selective configuration of switches to operate the transmitter and receiver circuitry in a recited mode. As a result, the rejection of claim 23 must likewise be withdrawn.

ARGUMENT 2: HEDBERG DOES NOT DISCLOSE A MULTI-MODE I/O CIRCUIT WHEREIN SAID TRANSMITTER CIRCUITRY SENDS DATA TO SAID RECEIVER CIRCUITRY IN ANOTHER IC OVER A FIRST PAIR OF ADJACENTLY DISPOSED CONDUCTORS, AND WHERE SAID RECEIVER CIRCUITRY RECEIVES DATA FROM SAID TRANSMITTER CIRCUITRY IN ANOTHER IC OVER A SECOND PAIR OF ADJACENTLY DISPOSED CONDUCTORS AS RECITED IN DEPENDENT CLAIMS 2, 14, AND 40.

In the office action of 11/30/2005, the Examiner asserted that "As per claims 2, 14, and 40, Hedberg disclosed the transmitter sends data to the receiver in another IC over a first pair of adjacently disposed conductors (fig. 5, fig. 6, col. 1/ln. 15-29, col. 5/ln. 42-col. 6/ln.8)."

Appellants respectfully note that claims 2, 14, and 40 depend on claims 1, 13, and 39, and, for the reasons discussed above, the rejections of claims 2, 14, and 40 must

likewise be withdrawn. In addition to the reasons discussed above, Appellants respectfully assert that the Examiner was in error when characterizing the recitations of claim of 2. Specifically, the Examiner asserts that Hedberg discloses a transmitter sending data to a receiver over a first pair of adjacently disposed conductors, while making no mention of any teaching of the receiver circuitry receiving data from the transmitter circuitry in another IC over a second pair of adjacently disposed conductors as recited in claim 2. In fact, Hedberg makes no such disclosure, either at the Exainer's citations or elsewhere. For this additional reason, the rejection of claim 2 must be withdrawn. As claims 14 and 40 recite similar language, the rejections of claims 14 and 40 must likewise be withdrawn.

<u>ARGUMENT 3: HEDBERG DOES NOT DISCLOSE A MULTI-MODE I/O CIRCUIT WHEREIN SAID TRANSMITTER CIRCUITRY AND SAID RECEIVER CIRCUITRY ARE SELECTIVELY CONFIGURED BY SWITCHES FOR OPERATING IN A MODE DEFINED BY A SINGLE DIFFERENTIAL VOLTAGE MODE LINK WITH A SINGLE-ENDED INPUT DRIVE AS DISCLOSED IN DEPENDENT CLAIMS 8 AND 46.</u>

In the office action of 11/30/2005, the Examiner asserted that "As per claims 8 and 46, Hedberg disclosed single differential voltage mode with single-ended input drive (fig. 5, fig. 6, col. 1/ln. 15-29, col. 5/ln. 42-col. 6/ln.8)." Appellants respectfully note that claims 8 and 46 both recite the selective configuration by switches of the transmitter and receiver circuitry. As a result, for the reasons discussed above, the rejections of claims 8 and 46 must likewise be withdrawn.

<u>ARGUMENT 4: HEDBERG DOES NOT DISCLOSE A MULTI-MODE I/O CIRCUIT WHEREIN THE TRANSMITTER CIRCUITRY AND THE RECEIVER CIRCUITRY ARE SELECTIVELY CONFIGURED BY SWITCHES FOR OPERATING IN A MODE DEFINED BY A SINGLE DIFFERENTIAL VOLTAGE MODE LINK WITH A DIFFERENTIAL INPUT DRIVE AS RECITED IN DEPENDENT CLAIMS 9, 20, AND 47.</u>

In the office action of 11/30/2005, the Examiner asserted that "As per claims 9, 20, and 47, Hedberg disclosed differential voltage mode with differential input drive (fig. 5, fig. 6, col. 1/ln. 15-29, col. 5/ln. 42-col. 6/ln.8)." Appellants respectfully note that claims 9, 20, and 47 all recite the selective configuration by switches of the transmitter and receiver circuitry and, for the reasons discussed above, the rejections of claims 9, 20, and 47 must likewise be withdrawn.

ISSUE B:

ARGUMENT 1: HEDBERG DOES NOT DOES NOT, ALONE OR IN COMBINATION WITH PENA-FINOL (5,832,370), TEACH OR SUGGEST TRANSMITTER CIRCUITRY AND RECEIVER CIRCUITRY SELECTIVELY CONFIGURED BY SWITCHES FOR OPERATING IN A CURRENT MODE LINK MODE AS RECITED IN CLAIMS 7, 10-11, 18-19, 21-22, 45, 48-49, AND 51.

The Examiner asserted that "As per claims 7, 10-11, 18-19, 21-22, 45, and 48-49, Hedberg does not disclose a current mode IC circuitry. However, such is well known in the art, as taught by Pena-Finol et al. (fig. 2-5, col. 2/ln. 10-col. 4/ln. 45). Therefore, it would have been obvious to one of ordinary skill in the art to provide such teaching of Pena-Finol et al. to the communication circuitry of Hedberg to avoid voltage variation and interference data transmission."

To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As held in In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494,496 (CCPA 1970), "All words in a claim must be considered in judging the patentability of that claim against the prior art." Appellants allow that Pena-Finol teaches, generally, communication between a transmitter circuit and a receiver circuit in a current mode. However, Pena-Finol does not teach, nor does the Examiner assert that Pena-Finol

teaches, an I/O circuit constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link as recited in independent claim 1, 13, and 39.

Appellants note that cited Figs. 2-4 illustrate differential output currents I_{203} and I_{204} which are further described at the Examiner's citation to the specification. Appellants further note that Fig. 5 does illustrate a single-ended input current I_{203}. Specifically, at the Examiner's citation of col. 4, lines 36-44, it is stated:

> The receiver 400 shown in FIG. 5 is a single-ended embodiment which receives a single-ended input current I_{203} at conductor 203 and produces a single-ended output voltage V_{OUT} at output terminal 512. Where the input current comprises a differential current having, for example, true and complementary components, a differential embodiment is readily provided by duplicating components 502-512. Components 502-512 process the true component of the differential input current and the duplicate circuit processes the complementary component.

As is evident, Pena-Finol does not teach an I/O circuit constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current mode links, and as a single differential current mode link as recited in claims 1, 13, and 39. Rather, Pena-Finol teaches the duplication of eleven components to form a duplicate circuit in order to receive a differential current. There is no teaching of transistors selectively interconnected by switches to operate in either mode as claimed. As neither Hedberg nor Pena-Finol teach this element of claims 1, 13, and 39, the combination of Hedberg and Pena-Finol, such a combination neither suggested nor deemed appropriate anywhere herein, likewise fails to teach this element. As a result, for this reason alone, the rejections of claims 1, 13, and 39 must be withdrawn.

Appellants respectfully assert that all of claims 7, 10-11, 18-19, 21-22, 45, and 48-49 recite the selective configuration by switches of the transmitter and receiver circuitry for operating the circuitry in various modes. As a result, for the reasons discussed above, the rejections of claims 7, 10-11, 18-19, 21-22, 45, and 48-49 must be withdrawn.

ISSUE B:

ARGUMENT 2: HEDBERG DOES NOT DOES NOT, ALONE OR IN COMBINATION WITH BJORK (6,009,314), TEACH OR SUGGEST A MULTI-MODE I/O CIRCUIT WHEREIN CERTAIN SWITCHES ARE PROVIDED TO CONVERT SAID I/O CIRCUITRY INTO EITHER SAID TRANSMITTER CIRCUITRY CONFIGURATION OR INTO SAID RECEIVER CIRCUITRY CONFIGURATION AS RECITED IN CLAIMS 12 AND 24.

The Examiner asserted that "As per claims 12 and 24, Hedberg does not disclose a transceiver IC. However, such is well known in the art, as taught by Bjork et al. (fig. 1). Therefore, it would have been obvious to one of obvious skill in the art to provide such circuitry of Bjork et al. to the communication circuitry of Hedberg to reduce the size of the radio equipment, more and more functionality is being incorporated onto a single integrated circuit chip." It is noted that, while the Examiner states that Hedberg does not disclose a transceiver IC, the Examiner above rejected claims 12 and 24 as being anticipated by Hedberg. Appellants arguments for the patentability of claims 12 and 24 are therefore discussed above.

Appellants here assert that Bjork et al. do not teach, nor does the Examiner assert otherwise, transistors selectively interconnected by switches to operate in either mode as claimed. As neither Hedberg nor Bjork et al. teach this element of, the combination of Hedberg and Bjork et al., such a combination neither suggested nor deemed appropriate anywhere herein, likewise fails to teach this element. As a result, for this reason alone, the

rejections of claims 12 and 24 must be withdrawn. Claim 50 recites language similar to that of claims 12 and 24 and, for the reasons discussed above, the rejection of claim 50 must be withdrawn.

ISSUE C:

ARGUMENT 1: CLAIMS 2, 14, AND 40 PROVIDE PROPER ANTECEDENT BASIS FOR "SAID OTHER IC".

The Examiner rejected claims 2, 14, and 40 for reciting "said other IC". The Examiner asserted that there is insufficient antecedent basis in the claims for the limitation. Applicants respectfully respond that the construction "said other IC" derives proper antecedent basis from the preceding recitation of "another IC". As a result, the rejections of claims 2, 14, and 40 must be withdrawn.

CONCLUSION

For at least the above reasons, the Appellants contend that all of independent claims 1, 13, and 39 are patentable over Hedberg, Pena-Finol, and Bjork et al., alone or in combination. As all of claims 2, 5-12, 14, 17-24, 40, and 43-51 are dependent upon claims 1, 13, and 39, they are likewise patentable. Appellants note that claims 3, 4, 15, 16, 41, and 42 are objected to and remain allowable subject to being rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Appellants respectfully request the Board reverse the final rejection in the Office Action of November 30, 2005, and further that the Board rule that the pending claims are patentable over the cited art.

Respectfully submitted:

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25 Sep 06
Date

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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(8) CLAIMS APPENDIX

1. (Previously Presented) A multi-mode Input/Output (I/O) circuit for transmitting and receiving data between integrated circuits (ICs), wherein each IC contains at least one of said I/O circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry sending data to receiver circuitry in another IC, and said receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

2. (Previously Presented) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in said other IC over a second pair of adjacently disposed conductors.

3. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

4. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

5. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

6. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended voltage mode link mode.

7. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended current mode link mode.

8. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

9. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

10. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

11. (Original) A multi-mode I/O circuit as in claim 1, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by single differential current mode link with a differential input drive.

12. (Original) A multi-mode I/O circuit as in claim 1, wherein certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

13. (Previously Presented) A method for transmitting and receiving data between integrated circuits (ICs) that comprise a portable radio communication device, comprising:

providing at least two ICs to each contain at least one I/O circuit, said I/O circuit comprising at least one of transmitter circuitry or receiver circuitry, the transmitter circuitry sending data to receiver circuitry in another IC, and the receiver circuitry receiving data from transmitter circuitry in another IC, the I/O circuit being constructed with CMOS-based transistors; and

selectively interconnecting together the CMOS-based transistors with switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

14. (Previously Presented) A method as in claim 13, wherein said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in said other IC over a second pair of adjacently disposed conductors.

15. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC

16. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of

double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

17. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a double single-ended voltage mode link mode.

18. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a double single-ended current mode link mode.

19. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

20. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

21. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

22. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by the switches for operating in a mode defined by single differential current mode link with a differential input drive.

23. (Original) A method as in claim 13, wherein said transmitter circuitry and said receiver circuitry are selectively configured by said switches for operating in one of said plurality

of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

24. (Original) A method as in claim 13, wherein certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

Claims 25-38: Cancelled

39. (Previously Presented) A device comprising a plurality of integrated circuits (ICs) and further comprising multi-mode Input/Output (I/O) circuit for transmitting and receiving data between at least two ICs, where each of the at least two ICs contains at least one of said I/O circuits, comprising at least one of transmitter circuitry or receiver circuitry, said transmitter circuitry sending data to receiver circuitry in another IC, and said receiver circuitry receiving data from transmitter circuitry in another IC, said I/O circuit being constructed with CMOS-based transistors that are selectively interconnected together by switches to operate as two single-ended, current or voltage mode links, and as a single differential current or voltage mode link.

40. (Previously Presented) A device as in claim 39, where said transmitter circuitry sends data to said receiver circuitry in another IC over a first pair of adjacently disposed conductors, and where said receiver circuitry receives data from said transmitter circuitry in said other IC over a second pair of adjacently disposed conductors.

41. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating under a condition where a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

42. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of a plurality of double single-ended, CMOS voltage level link modes, wherein in a first mode a power supply voltage of said transmitter circuitry is equal to a power supply voltage of said receiver circuitry in another IC, wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in another IC, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in another IC.

43. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in one of said plurality of double single-ended, CMOS voltage level link modes, or in said differential voltage or current mode links, and wherein the ICs at each end of the link may operate with different supply voltages.

44. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended voltage mode link mode.

45. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a double single-ended current mode link mode.

46. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

47. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential voltage mode link with a differential input drive.

48. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by a single differential current mode link with a single-ended input drive mode.

49. (Previously Presented) A device as in claim 39, where said transmitter circuitry and said receiver circuitry are selectively configured by switches for operating in a mode defined by single differential current mode link with a differential input drive.

50. (Previously Presented) A device as in claim 39, where certain switches are provided to convert said I/O circuitry into either said transmitter circuitry configuration or into said receiver circuitry configuration.

51. (Previously Presented) A device as in claim 39, where at least one of said plurality of ICs comprises a radio frequency IC, and where at least one other one of said ICs comprises a baseband IC.

END OF CLAIMS

(9) EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by Appellant.

(10) RELATED PROCEEDING APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 C.F.R. §41.37.